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Patent No.: 7,130,333 B2
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Application No.: 09/995,095
Applicant(s): Gibson, Jr. et al.
Filed: 11/27/2001
Title: Method And Device For frame Sync Detection Using Channel Combining and Correlation
Attorney Docket No.: 907A.0081.U1(US)
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Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Request For Certificate of Correction
(Office Mistake)
35 U.S.C. §254 (37 C.F.R. §1.322)

Sir:

This is a request for a Certificate of Correction (MPEP 1480) in regard to the above-identified patent. Attached is a Form PTO-1050. The mistakes, incurred through the fault of the Patent and Trademark Office, are clearly disclosed by the records of the Office as indicated by the following description:

In Claim 8: Column 6, line 12, "sciuared" should be deleted and --squared-- should be inserted. In claim 8 of Amendment filed June 27, 2006, the claim was correctly written.

In Claim 11: Column 6, line 57, "sciuared" should be deleted and --squared-- should be inserted. In claim 11 of Amendment filed June 27, 2006, the claim was correctly written.

In Claim 14: Column 7, line 16, "sciuared" should be deleted and --squared-- should be inserted. In claim 14 of Amendment filed June 27, 2006, the claim was correctly written.

The Office is requested to issue a Certificate of Correction.

Respectfully submitted,

Harry Smith 11/8/2006

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail on the date shown below in an envelope addressed to: Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

11/8/2006
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NOV 1 5 2006

square root of the output of adder **211** could be taken in order to provide other system processing information.

If the summed columns from the I_{1-n} and Q_{1-n} data streams do not correspond to the sync word **26** then the accumulated value will be below a predetermined threshold and a no sync condition would be declared **39**. Alternatively, if the summed columns from the I_{1-n} and Q_{1-n} data streams do correspond to the sync word **26** then the accumulated value will be relatively large and if the sum of the squares exceeds the predetermined threshold then comparator **213** outputs sync detect signal and frame sync is declared **30**.

It should be understood that the foregoing description is only illustrative of the invention. Moreover, it will be readily appreciated that an advantage of the present invention is the use of multiple channels to detect frame sync. It will be further appreciated that advantages of the present invention include an effective increase of approximately 12 dB in the power level of the sync word (for a 16-bit sync word and twenty input channels I_1–I_{20} and Q_1–Q_{20}). In addition, various alternatives and modifications can be devised by those skilled in the art without departing from the invention. Accordingly, the present invention is intended to embrace all such alternatives, modifications and variances that fall within the scope of the appended claims.

What is claimed is:

1. A method for frame sync detection using signal combining and correlation, the method comprising the steps of:

despreading PN coded signals to provide in-phase I_1–I_n, and quadrature phase Q_1–Q_n signals, wherein each I_1–I_n and each Q_1–Q_n signal contains at least one sync bit and where $n \geqq 2$;

summing the at least one sync bit from each I_1–I_n, and quadrature phase Q_1–Q_n signals to form sums I_{s1} and Q_{s1}, respectively;

providing a reference sync, wherein the reference sync comprises at least one bit;

comparing each sum I_{s1} and Q_{s1} with the at least one bit from the reference sync;

accumulating the results of each I_{s1} and Q_{s1} comparison so as to form two accumulates, I_A and Q_A, respectively;

squaring each accumulate $I_{A\ and\ QA}$, respectively, to form I_A^2 and Q_A^2;

summing I_A^2 and Q_A^2; and

comparing $I_A^2+Q_A^2$ with a predetermined threshold and as a result of the comparison, making a determination whether frame sync has been achieved is made.

2. A method as in claim **1**, wherein the step of despreading PN coded signals to provide in-phase I_1–I_n and quadrature phase Q_1–Q_n signals further comprises the step of letting n=20.

3. A method as in claim **1**, wherein the step of summing the at least one sync bit from each I_1–I_n and quadrature phase Q_1–Q_n signals to form sums I_{s1} and Q_{s1}, respectively, further comprises the step of forming sixteen sync bit sums from each I_1–I_n and quadrature phase Q_1–Q_n signals.

4. A method as in claim **3**, wherein the step of providing the reference sync further comprises the step of providing a sixteen-bit reference sync.

5. A method as in claim **1**, wherein the step of providing the reference sync further comprises the step of storing the reference sync in a local accessible memory.

6. A method as in claim **1**, wherein the step of providing the reference sync further comprises the step of receiving the reference sync from a remote source.

7. A method as in claim **1**, wherein the step of summing I_A^2 and Q_A^2 further comprises the steps of:

performing a square root operation on the sum $I_A^2+Q_A^2$; and

comparing the square root of the sum $I_A^2+Q_A^2$ with the predetermined threshold value.

8. A device comprising:

a channel despreader, wherein the channel despreader provides at least two each in-phase I1–In and, quadrature phase Q1–Qn channels, where $n \geqq 2$;

at least one I-sync processor, wherein the at least one I-sync processor is coupled to the channel despreader, the at least one I-sync processor receiving I1–In data streams and providing an accumulated sciuared value I_A as an output; Squared

at least one Q-sync processor, wherein the at least one Q-sync processor is coupled to the channel despreader, the at least one Q-sync processor receiving Q1–Qn data streams and providing an accumulated squared value Q_A as an output;

a first summer connected to the I-sync processor and the Q-sync processor to add the accumulated squared value I_A and the accumulated squared value Q_A to form a sum; and

a comparator, wherein the comparator is coupled to the first summer and compares the sum to a predetermined threshold, wherein the comparator compares a sum from the first summer with a predetermined threshold and, as a result of the comparison, a determination whether frame sync has been achieved is made.

9. A device as in claim **8** wherein the channel despreader comprises a direct sequence spread spectrum (DSSS) despreader.

10. A device as in claim **8** wherein the channel despreader comprises a frequency hop spread spectrum (FHSS) despreader.

11. A device as in claim **8** wherein the at least one I-sync processor comprises:

a first I-binary adder;

a first I-memory device, the first I-memory device coupled to the first I-binary adder;

a reference sync;

a first I-multiplier, wherein the first I-multiplier multiplies the reference sync with the output of the first I-memory device to provide an I-multiplier result;

a first I-accumulator, wherein the first accumulator comprises:

a first I-register bank;

a second I-adder, the second I-adder having at least two inputs, wherein one of the two inputs is coupled to an output of the first I-register bank;

a second I-register bank, wherein an output of the second I-register bank is coupled to an input of the second I-adder; and

a first I-squaring device, wherein the first I-squaring device is coupled to the output of the second I-register bank, wherein the first I-accumulator receives the I-multiplier result from the first I-multiplier and provides a sciuared accumulated I value. Squared

12. A device as in claim **11** wherein the first I-binary adder comprises a two's-complement adder.

13. A device as in claim **11** wherein the first I-memory device comprises a first dual port 16×16 RAM.

14. A device as in claim **8** wherein the at least one Q-sync processor comprises:

a first Q-binary adder;

a first Q-memory device, the first Q-memory device coupled to the first Q-binary adder;

a first Q-multiplier, wherein the first Q-multiplier multiplies the reference sync with the output of the first Q-memory device to provide a Q-multiplier result;

a first Q-accumulator, wherein the first Q-accumulator comprises:

a first Q-register bank;

a second Q-adder, the second Q-adder having at least two inputs, wherein one of the two inputs is coupled to an output of the first Q-register bank;

a second Q-register bank, wherein an output of the second Q-register bank is coupled to an input of the second Q-adder; and

a first Q-squaring device, wherein the first Q-squaring device is coupled to the output of the second Q-register device, wherein the first Q-accumulator receives the Q-multiplier result and provides a sciuared accumulated Q value. squared

15. A device as in claim **14** wherein the first Q-binary adder comprises a two's-complement adder.

16. A device as in claim **14** wherein the first Q-memory device comprises a first dual port 16×16 RAM.

17. An integrated circuit (IC), wherein the integrated circuit comprises:

a channel despreader, wherein the channel despreader provides at least two each in-phase I1–In and, quadrature phase Q1–Qn channels, where n≧2;

at least one I-sync processor, wherein the at least one I-sync processor is coupled to the channel despreader, the at least one I-sync processor receiving I1–In data streams and providing an accumulated squared value I_A as an output;

at least one Q-sync processor, wherein the at least one Q-sync processor is coupled to the channel despreader, the at least one Q-sync processor receiving Q1–Qn data streams and providing an accumulated squared value Q_A as an output;

a first summer connected to the I-sync processor and the Q-sync processor to add the accumulated squared value I_A and the accumulated squared value Q_A to form a sum; and

a comparator, wherein the comparator is coupled to the first summer and compares the sum to a predetermined threshold, wherein the comparator compares a sum from the first summer with a predetermined threshold, and as a result of the comparison, a determination whether frame sync has been achieved is made.

18. An IC as in claim **17** wherein the IC comprises an Application Specific IC (ASIC).

19. An IC as in claim **17** wherein the IC comprises a field programmable gate array (FPGA).

20. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for frame sync detection using signal combining and correlation, the method comprising the steps of:

despreading PN coded signals to provide in-phase I_1–I_n, and quadrature phase Q_1–Q_n signals, wherein each I_1–I_n and each Q_1–Q_n signal contains at least one sync bit and where n≧2;

summing the at least one sync bit from each I_1–I_n, and quadrature phase Q_{1-Qn} signals to form sums I_{s1} and Q_{s1}, respectively;

providing a reference sync, wherein the reference sync comprises at least one bit;

comparing each sum I_{s1} and Q_{s1} with the at least one bit from the reference sync;

accumulating the results of each I_{s1} and Q_{s1} comparison so as to form two accumulates, I_A and Q_A, respectively;

squaring each accumulate I_A and Q_A, respectively, to form I_A^2 and Q_A^2;

summing I_A^2 and Q_A^2; and

comparing $I_A^2+Q_A^2$ with a predetermined threshold and as a result of the comparison, making a determination of whether frame sync has been achieved is made.

21. A program storage device as in claim **20** wherein the program of instructions comprise at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file.

22. A device as in claim **8** wherein the device provides non-coherent power detection.

23. An integrated circuit as in claim **17** wherein the device provides non-coherent power detection.

24. A device comprising:

a channel despreader, wherein the channel despreader provides at least two each in-phase I1–In and, quadrature phase Q1–Qn channels, where n≧2;

at least one I-sync processor, wherein the at least one I-sync processor is coupled to the channel despreader, the at least one I-sync processor receiving I1–In data streams and providing an accumulated I_A squared value as an output;

at least one Q-sync processor, wherein the at least one Q-sync processor is coupled to the channel despreader, the at least one Q-sync processor receiving Q1–Qn data streams and providing an accumulated Q_A squared value as an output;

a first summer connected to the I-sync processor and the Q-sync processor to add the accumulated I_A squared value and the accumulated Q_A squared value to form a sum; and

a comparator, wherein the comparator is coupled to the first summer and compares the sum to a predetermined threshold, wherein the device provides non-coherent power detection.

25. An integrated circuit (IC), wherein the integrated circuit comprises:

a channel despreader, wherein the channel despreader provides at least two each in-phase I1–In and quadrature phase Q1–Qn channels, where n≧2;

at least one I-sync processor, wherein the at least one I-sync processor is coupled to the channel despreader, the at least one I-sync processor receiving I1–In data streams and providing an accumulated I_A squared value as an output;

at least one Q-sync processor, wherein the at least one Q-sync processor is coupled to the channel despreader, the at least one Q-sync processor receiving Q1–Qn data streams and providing an accumulated Q_A squared value as an output;

a first summer connected to the I-sync processor and the Q-sync processor to add the accumulated I_A squared value and the accumulated Q_A squared value to form a sum; and

a comparator, wherein the comparator is coupled to the first summer and compares the sum to a predetermined threshold, wherein the integrated circuit provides non-coherent power detection.

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,130,333 B2

DATED : October 31, 2006

INVENTOR(S) : Leroy Andrew Gibson, Jr., Dan M. Griffin, Lyman D. Horne, Randal R. Sylvester

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

IN THE CLAIMS:

Claim 8, Column 6, line 12, Please delete "sciuared" and replace with --squared--.

Claim 11, Column 6, line 57, Please delete "sciuared" and replace with --squared--.

Claim 14, Column 7, line 16, Please delete "sciuared" and replace with --squared--.

MAILING ADDRESS OF SENDER (Please do not use customer number

PATENT NO. 7,130,333 B2

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